Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method comprising:

representing each vector associated with an integrated circuit datapath design as one of a row and a column in a graphical interface; and

representing each bit slice associated with the integrated circuit datapath design in an orthogonal manner to the vectors in the graphical interface, the corresponding vector and bit slice representation in the graphical interface being different than an associated physical layout.

2. (Original) The method of claim 1 further comprising:

using similar visual representations to indicate cell similarities.

3. (Original) The method of claim 1 wherein

representing each vector includes representing each vector as a row, and wherein

representing each bit slice includes representing each bit slice as a column.

4. (Currently Amended) The method of claim 1 further comprising:

representing information indicating connectivity between a selected vector and at least one of another vector and [[and]] interface pins.

5. (Original) The method of claim 4 further comprising:

providing drag and drop editing capabilities to move a vector.

6. (Original) The method of claim 5 wherein,

each vector includes a plurality of cell instances, and wherein,

providing drag and drop editing capabilities includes providing drag and drop editing capabilities to move a group of cell instances.

7. (Original) An apparatus comprising:

a vector extraction engine to extract vectors from an input file associated with an integrated circuit design; and

a vector editor to provide a graphical interface to represent and edit the extracted vectors as one of a row and a column and to represent bit slices in an orthogonal manner to the extracted vectors.

8. (Original) The apparatus of claim 7 wherein

the graphical interface is further to represent similar cells associated with the integrated circuit design using a similar visual representation.

9. (Original) The apparatus of claim 8 wherein

the vector extraction engine is to extract vectors using a name-based vector extraction approach.

10. (Original) The apparatus of claim 8 wherein

the vector extraction engine is to extract vectors using a bus/connectivity-based vector extraction approach.

11. (Original) The apparatus of claim 7 wherein

the graphical interface is further to represent similar cells associated with the integrated circuit design using a similar color and stippling.

12. (Original) The apparatus of claim 7 wherein

the vector editor is further to assign one of a plurality of predetermined visual representations to each cell type associated with the integrated circuit design.

13. (Original) The apparatus of claim 12 wherein

the vector editor is further to visually represent connectivity information indicating connections between a vector and one of another vector and an interface pin.

14. (Original) The apparatus of claim 13 wherein

the graphical interface is further to provide drag and drop editing capabilities to move one or more of vectors, bit slices, and connections.

15. (Original) The apparatus of claim 14 wherein

the vector editor is to provide data to a placement engine, the placement engine to output a datapath placement associated with the integrated circuit design.

16. (Original) The apparatus of claim 15 wherein

the vector editor is further to provide at least one metric indicating a quality of the data provided by the vector editor.

17. (Original) The apparatus of claim 7 wherein

the vector editor provides at least one of an auto-merge and an auto-align command.

18. (Previously Presented) A computer-accessible storage medium storing information that, when accessed by a machine, causes the machine to:

represent vectors associated with an integrated circuit datapath design in one of a row and a column in a graphical interface; and

represent bit slices associated with the integrated circuit datapath design in an orthogonal manner in the graphical interface, wherein the manner in which

the vectors and bit slices is represented in the graphical interface is different than an associated physical layout.

19. (Original) The computer-accessible storage medium of claim 18 further storing information that, when accessed by a machine, causes the machine to:

represent connectivity between a vector and one of another vector and an interface pin.

20. (Original) The computer-accessible storage medium of claim 19 further storing information that, when accessed by a machine, causes the machine to:

extract the vectors from an input file associated with the integrated circuit datapath design.

21. (Original) The computer-accessible storage medium of claim 20 wherein

extracting the vectors from the input file includes using a name-based extraction approach.

22. (Original) The computer-accessible storage medium of claim 20 wherein

extracting the vectors from the input file includes using a bus/connectivity-based extraction approach.

23. (Previously Presented) An apparatus comprising:

a vector editor to represent vectors associated with an integrated circuit datapath design as one of rows and columns and bit slices associated with the integrated circuit datapath design in an orthogonal manner in a graphical interface, wherein the row and column representation is different than an associated physical layout,

the vector editor to provide one of an auto-merge and an auto-align command to operate on the vectors; and

a placement engine to receive an output of the vector editor and to produce an associated placement.

24. (Original) The apparatus of claim 23 wherein,

the vector editor is further to use similar visual representations to identify similar cell instances.

25. (Original) The apparatus of claim 24 wherein,

similar visual representations includes a combination of a similar color and a similar stippling technique.

26. (Original) The apparatus of claim 23 wherein,

the vector editor provides drag and drop editing capabilities to edit the vectors, bit slices and associated connectivity.